IN THE SPECIFICATION:

MLB 7/24/06 The paragraph beginning on page 2 line 24 is amended as follows:

These and other objective are achieved in the present invention by providing an integrated circuit with an on-chip jitter measurement circuit. The on-chip jitter measurement circuit comprises a plurality of delay elements, a first set of circuitry and a second set of circuitry. The delay elements each have an associated delay, an input configured to receive an input clock signal and an output responsive to the associated delay and [[the]] input clock signal. The input clock signal has a significant instant. The first set of circuitry is connected to the inputs and outputs of the plurality of delay elements. Moreover, the first set of circuitry is also configured to detect the significant instant [[on]] of the input clock signal. The first set of circuitry is also configured to output a signal responsive to the significant instant [[on]] of the input clock signal. The second set of circuitry is configured to receive the signal responsive to the significant instant [[on]] of the input clock signal and a first trigger signal. Also, the second set of circuitry is configured to latch onto the signal responsive to the significant instant [[on]] of the input clock signal and is further responsive to a significant instant [[on]] of the first trigger signal. A measure for jitter is determined from the latched signal responsive to the significant instant [[on]] of the input clock signal.

The paragraph beginning on page 3 line 5 is amended as follows:

In another embodiment of the invention, the latched signal is filtered. In yet another embodiment, latched signal is recorded for a plurality of significant instants [[on]] of the first trigger signal. In another embodiment of the invention, a result calculator is configured to provide information collected from the measure of jitter.

The paragraph beginning on page 3 line 9 is amended as follows:

A method is also disclosed for measuring jitter of a significant instant [[on]] of an input clock signal derived from a reference clock signal. The method comprises the steps of receiving an input clock signal, delaying the input clock signal, receiving a trigger